REMARKS

In the Office Action mailed January 15, 2002, claims 1, 28, 37-48, 52-59, 102, 143, 144, 146, 147 and 210-222 are pending in the application.

Claims 53 and 220 have been amended to correct informalities.

Claims 44, 46, 59 and 218 have been amended to point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 28, 37-39, 41, 53, 58, 102, 210-212, 217, 218 and 220 were rejected under 35 U.S.C. 102(b) as being anticipated by Zappe. (USP 3,983,546).

Claims 102, 143, 144, 217, 218, 221 and 222 were rejected under 35 U.S.C. 102(b) as being anticipated by Ballmer et al. (USP 4,876,535).

Claims 1, 28, 37-39, 41, 42, 58, 102, 210-212 and 217-220 were rejected under 35 U.S.C. 102(e) as being anticipated by Jacobsen (USP 5,673,131 and 5,269,882 hereinafter '131 and '882).

Claims 40, 43, 45, 47, 54 and 55 were rejected under 35 U.S.C. 103(a) as being unpatentable over Zappe.

Claims 40 and 45 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobsen '131.

Claims 53-55 were rejected under 35 U.S.C. 101(a) as being unpatentable over Jacobsen '131 in view of Zappe.

Claims 44 and 59 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph as set forth in the Office Action.

Claim 46 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph as set forth in the Office Action and to include all of the limitations of the base claim and any intervening claims.

Claims 48, 52, 56, 57 and 213-216 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants wish to express their thanks to the Examiner for the obvious care with which he has reviewed the text of the claims.

Claims 53 and 220 have been amended to correct typographical errors noted by the Examiner. Claims 44, 46 and 59 have been revised as suggested by the Examiner to overcome the rejections under 35 U.S.C. 112, 2d paragraph. Claim 218 has been revised by deleting the phrase to which the Examiner objects.

With these changes it is believed that 44, 46, 59 and 218 are in condition for allowance.

The applicants note the Examiner's indication that claims 48, 52, 56, 57, and 213-216 would be allowable if rewritten in independent form.

Applicants submit that claims 146 and 147, which were not specifically addressed in the Office Action, are patentable for the same reason claim 57 is patentable.

In addition to the amendments to claims 44, 46, 53, 59, 218 and 220 discussed above, claims 1, 28 and 102 have been amended.

In addition, several new claims have been added. Before discussing these claims, a brief review of applicants' invention and the cited art is desirable.

Applicant's claimed invention relates to an apparatus for communicating or signalling between integrated circuit (IC) chips, modules or substrates using capacitive coupling rather than conductive paths. For example, in large part, the need for multichip modules arises from the inability of the prior art to produce arbitrarily large semiconductor dies with acceptable yield as well as the high cost of wiring on semiconductor dies. Such problems have forced designers to partition large systems among multiple dies. To effect signalling between different chips and modules, the prior art requires the use of conductive connectors, solder bumps, wire-bond interconnections or the like. Unfortunately, such means introduces significant latency, frequency limitations and power requirements. To mitigate these problems, the present invention effects signalling capacitively. As described beginning at page 25, line 16, pairs of half-capacitor plates (Fig. 1, elements 13, 14), one half located on each IC chip (11), module or substrate (10), are used to capacitively couple signals from one IC chip, module or substrate to another. The use of such plates relaxes the area needed to effect signalling, and reduces or eliminates the requirements for exotic metallurgy.

Zappe discloses Josephson tunneling devices that are used as parametrons. With reference to Fig. 14, Zappe states at col. 12, lines 58-67:

> In operation, conductive plates 170A and 170B are capacitively coupled and transmit information there-between at a frequency F_1. In the same manner, information is transmitted between conductive plates 172A and 172B at a frequency F_2. At the frequencies used for Josephson circuitry (10^{11} - 10^{12} Hz) capacitive coupling between conductive plates located on separate circuit chips is sufficient to provide communication between the chips without the requirement for interconnecting wires.

It is to be noted that Josephson Junction circuits are superconducting circuits, not semiconducting circuits.

Ballmer discloses a data carrier such as a smartcard and a data reader. Planar electrodes 11, 16 and 12, 17 are used to capacitively couple signals from the data reader to the card and back to the reader. Various circuits are shown on the data carrier including resistors, switches, microprocessors and memory. In addition, as shown in Figs. 5-7, AC power may be coupled to the data carrier where it is rectified by a diode bridge D1-D4. As the Examiner appreciates, Ballmer does not disclose or suggest the use of capacitive coupling to connect signals between a die and a substrate.

Jacobsen discloses a three-dimensional circuit structure. The preferred structures appear to be cylindrical structures such as fiber optic strands. Circuits are described as being formed on the surface of such structures using non-planar exposure beam lithography. In conjunction with Fig. 9B of the '131 patent, Jacobsen describes capacitive coupling between capacitor plates such as elements 214 and 216 on cylindrical substrates 212, 210, respectively.

Independent claims 1 and 28 both recite a "chip." At page 183, *The New IEEE Standard Dictionary of Electrical and Electronic Terms* (IEEE, 5th Ed., January 15, 1993) defines a chip as "A small unpackaged functional element made by subdividing a wafer of semiconductor material. Sometimes referred to as a 'die.'" A copy of page 183 is enclosed.

In view of the foregoing definition, it would appear that the word "chip" is well understood in the industry to refer to a semiconductor. Nevertheless, to make clear that the chip referred to is a semiconductor, claims 1 and 28 have been amended to recite a "semiconductor chip."

Claims 1 and 28 are believed to define over Zappe because Zappe does not disclose a semiconductor device. Rather, his Josephson devices are superconductors. Superconductors

are very different from semiconductors. Zappe is interested in new applications for Josephson tunneling devices and, in particular, in the use of such devices at very high frequency parametrons. In addition, he is interested in the use of Josephson tunneling devices or circuit interconnection. He states at Col. 1, lines 35-37 that:

> "The prior art has also not addressed the problem of interconnections between circuit chips having circuits thereon for memory and logic functions. Such functions could be performed by Josephson tunneling devices or by other electrical components."

But Zappe does not in fact solve this prior art problem. There are no Josephson tunneling devices that work as memories, i.e., that latch (hold) a binary value. And, all logic devices formed with Josephson devices are likewise limited to the non-latching variety.

Furthermore, by the phrase "other electrical components," Zappe turns out to mean solely alternatives which are themselves Josephson tunneling electrical components. Zappe offers no further disclosure whatsoever regarding circuit chips other than those containing superconducting Josephson tunneling devices and operating at cryogenic temperatures. Zappe never teaches or describes any logic, memory, or other electrical components which are non superconducting, much less semiconducting. He is simply silent on the subject of non-superconducting components.

Zappe's failure to deal with non-superconducting electronics is important because the circuit topologies and logic gates needed to enable a superconducting version are in every case incompatible with the non-superconducting versions. Teaching an apparatus for superconducting does not teach the non-superconducting circuit. Enabling an apparatus for superconducting does not enable the non-superconducting circuit. The two technologies are not analogous. Nothing in Zappe's patent would have changed if semiconductors had never come along.

Specifically, the Josephson tunneling devices he describes are Josephson oscillators, which have no non-superconducting equivalent; and parametrons, which measure minute changes in magnetic flux density. Since magnetic flux density is approximately one millionth as energetic as electric current, the semiconductor analog of a parametron is neither practical

or feasible. Superconducting Josephson tunneling junctions can nevertheless detect such small magnetic changes. However, superconducting circuits cannot latch (retain) a logic state; also, superconducting circuits do not impart gain. As a result, superconducting circuits are vastly different from the latching, semiconductor configurations claimed in claims 1 and 28 and disclosures in one technology do not suggest the other.

Claim 102 has been amended to recite that the first module has a plurality of semiconductor electronic devices. It is believed patentable over Zappe for the same reason claims 1 and 28 are patentable.

Dependent claims 37-43, 45-48, 52-58, 210-216 are believed patentable over Zappe for the same reason claim 1 is patentable.

Dependent claims 143-147 and 217-222 are believed patentable over Zappe for the same reason claim 102 is patentable.

Claim 102 has also been amended to recite "contacts for supplying DC power to said first module from a source outside said first module." As amended, claim 102 defines over Ballmer who teaches only a capacitive coupling for applying AC power to the data carrier. The entire emphasis in Ballmer is on non-contact transmission of information (Col. 1, line 45) and of energy (col. 1, line 48). There is no suggestion in Ballmer of a combination of modalities in which signals are transmitted by capacitive coupling and power is provided by contacts between a module and an external power source. Moreover, there is no suggestion in Ballmer of provision of DC power from outside the module.

For these reasons, claim 102 as amended is believed to be patentable over Ballmer. Likewise, dependent claims 143-147 and 217-222 are believed patentable.

With respect to Jacobsen, the Examiner has taken the position that the cylindrical substrates of Jacobsen are cylindrically shaped chips and has rejected many of the claims that recite chips as anticipated by Jacobsen under 35 U.S.C. 102(e). Applicants must respectfully disagree. It is apparent that the substrates of Fig. 9B of Jacobsen are cylinders such as optical fibers and not chips. The substrates are three-dimensional objects that plainly were not formed from a wafer and plainly were not made by subdividing a wafer. The differences between the structure and operation of the three-dimensional devices of Jacobsen and conventional planar

devices constitute the point of novelty between Jacobsen and the prior art as set forth in his patents and his file wrappers.

Accordingly, claims 1 and 28 define over Jacobsen in reciting semiconductor chips that are capacitively coupled to substrates. Nor does Jacobsen suggest capacitive coupling of chips to substrates. Jacobsen's cylinders are three-dimensional objects with shapes very different from those of chips. Whatever might work with Jacobsen's cylinders does not suggest what will work in the case of a chip on a substrate. For these reasons, claims 1 and 28 are believed to be patentable over Jacobsen.

Dependent claims 37-43, 45-48, 52-58 and 210-216 are believed patentable over Jacobsen for the same reason, claim 1 is patentable.

Independent claim 102 as amended recites contacts for providing DC power to the semiconductor electronic devices on the first module from an external source. Jacobsen does address how the substrates of Fig. 9B are to be powered. Accordingly, he does not suggest the structure of claim 102 where signaling between modules is accomplished by capacitive coupling and DC power is supplied by contacts.

Dependent claims 143-147 and 216-222 are believed patentable for the same reason claim 102 is patentable.

Claims 223 and 224 have been added to the application and are believed patentable for the same reason claim 28 is patentable.

Applicants wish to bring to the Examiner's attention the patents and other documents cited in U.S. Patent No. 6,362,972, a copy of which is enclosed.

In view of the foregoing, applicants believe that all of the claims are now in condition for allowance and respectfully requests the Examiner to pass the subject application to issue and to apply the Issue Fee previously paid on June 26, 2001 to the present application. If for any reason the Examiner believes any of the claims are not in condition for allowance, he is encouraged to phone the undersigned at (650) 849-7777 so that any remaining issues may be resolved.

Aside from the fee for the petition for extension of time, no additional fee is believed due for filing this response. However, if a fee is due, please charge such fee to Pennie & Edmonds LLP's Deposit Account No. 16-1150.

Respectfully submitted,

Date: July 15, 2002

Gary S. Williams (Reg. No. 31,066)
for Francis E. Morris (Reg. No. 24,615)
Pennie & Edmonds LLP
1155 Avenue of the Americas
New York, NY 10036
Telephone: (650) 849-7777

APPENDIX A

Changes to the Claims

1. (Amended) A modular electronic system comprising:

a substrate;

a semiconductor chip;

means for powering said chip;

means for capacitively signalling between said chip and said substrate; and

signal leads connected on said substrate and said chip to said means for capacitively signalling.

28. (Amended) An electronic system comprising:

a semiconductor chip;

a substrate;

a plurality of electronic devices implemented on said chip, a signal lead of at least one of said plurality of electronic devices coupled to a first half-capacitor attached to said chip; and,

a second half-capacitor attached to said substrate and capacitively coupling a signal to said first half-capacitor.

44. (Amended) A modular electronic system comprising:

a substrate;

a chip;

means for powering said chip;

means for capacitively signaling between said chip[s] and said substrate comprising first and second coupled half-capacitors, said first half-capacitor being associated with said chip and said second half-capacitor being associated with said substrate, said first and second coupled half-capacitors comprising effectively overlapping conductive regions separated by a gap that is at least partially filled with a dielectric; and

a power connector extending through said dielectric.

46. (Amended) A modular electronic system as defined in claim 45 wherein said dielectric has a substantially greater dielectric [factor] constant than does said passivation.

53. (Amended) A modular electronic system as defined in claim 39 further [a] comprising a plurality of coupled half-capacitors, a substantial area of said chip and a substantial portion of the area of said substrate overlapping said chip being covered with substantially overlapping half-capacitors.

59. (Amended) A modular electronic system comprising:

a substrate;

a chip;

means for powering said chip;

means for capacitively signaling between said chip[s] and said substrate comprising first and second coupled half-capacitors, said first half-capacitor being associated with said chip and said second half-capacitor being associated with said substrate, said first and second coupled half-capacitors comprising effectively overlapping conductive regions separated by a gap; and

an additional half-capacitor associated with one of said chip and said substrate.

102. (Amended) A modular electronic system comprising:

a first module having a plurality of semiconductor electronic devices, a first half-capacitor and at least one signal lead connecting said electronic devices to said first half-capacitor; [and]

a second module having a second half-capacitor, said modules being positioned such that said first and second half-capacitors provide a capacitive signal path between said first and second modules; and

contacts for supplying DC power to said first module from a source outside said first module.

218. (Amended) A modular electronic system as defined in claim 102 wherein said first module is positioned relative to said second module by motion transverse to said capacitive signal path [transverse to said conductive connection].

220. (Amended) A modular electronic system as defined in claim 102 wherein said first [nodule] module further includes a transmission line that is connected to a plurality of transmission lines.

--223. (New) A modular electronic system comprising:

a substrate;

a semiconductor chip;

a first half-capacitor attached to said semiconductor chip;

a plurality of electronic devices implemented on said chip, a signal lead of at least one of said plurality of electronic devices coupled to said first half-capacitor; and

a second half-capacitor attached to said substrate and capacitively coupling a signal to said first half-capacitor.

224. (New) The modular electronic system of claim 223 further comprising contacts for supplying DC power to said semiconductor chip from a source outside said chip.--